Preliminary Program for ICFEM 2016 Main Conference

Wednesday, 16 November 2016

9:00 ~ 9:15 Opening

9:15 ~ 10:15 Keynote

W. Eric Wong
Combinatorial Testing and Its Applications

10:15 ~ 10:45 Coffee break

10:45 ~ 12:15 Testing/Symbolic Execution

Weikai Miao, Geguang Pu, Yinbo Yao, Ting Su, Danzhu Bao and Yang Liu
Automated Requirements Validation for ATP Software via Specification Review and Testing

Takaya Saeki, Fuyuki Ishikawa and Shinichi Honiden
Automatic Instance Generation for Validating Alloy Models

Dominic Scheurer, Reiner Hähnle and Richard Bubel
A General Lattice Model for Merging Symbolic Execution Branches

12:15 ~ 14:00 Lunch

14:00 ~ 16:00 Hybrid/Service-Based Systems

Ryo Yanase, Tatsunori Sakai, Makoto Sakai and Satoshi Yamane
A Case Study of Formal Approach to Dynamically Reconfigurable Systems by Using Dynamic Linear Hybrid Automata

Richard Banach and Michael Butler
Modelling Hybrid Systems in Event-B and Hybrid Event-B: A Comparison of Water Tanks
Guillaume Babin, Yamine Ait Ameur, Neeraj Kumar Singh and Marc Pantel,
*A System Substitution Mechanism for Hybrid Systems in Event-B*

Manman Chen, Tian Huat Tan, Jun Sun, Jingyi Wang, Yang Liu, Jing Sun and Jin Song Dong
*Service Adaptation with Probabilistic Partial Models*

16:00 ~16:30 **Coffee break**

16:30 ~ 18:00 **Security**

Linas Laibinis, Elena Troubitsyna, Inna Pereverzeva, Ian Oliver and Silke Holtmanns
*A Formal Approach to Identifying Security Vulnerabilities in Telecommunication Networks*

Minh Hai Nguyen, Quan Thanh Tho and Le Duc Anh
*Multi-Threaded On-the-fly Model Generation of Malware with Hash Compaction*

Marco Rocchetto and Nils Ole Tippenhauer
*CPDY: Extending the Dolev-Yao Attacker with Physical-Layer Interactions*

Thursday, 17 November 2016

9:00 ~ 10:00 **Keynote**

Tom Maibaum
*A (Proto) Logical Basis for the Notion of a Structured Argument in a Safety Case*

10:00 ~ 10:30 **Coffee break**

10:30 ~ 12:30 **Formal Verification**

Francesco Marconi, Marcello M. Bersani, Madalina Erascu and Matteo Rossi
*Towards the formal verification of data-intensive applications through metric temporal logic*

Alexei Iliasov, Alexander Romanovsky and Paulius Stankaitis
*Proving Event-B models with reusable generic lemmas*

Waqar Ahmed and Osman Hasan
*Formal Availability Analysis using Theorem Proving*
Akira Tanaka, Reynald Affeldt and Jacques Garrigue
Formal Verification of the rank Algorithm for Succinct Data Structures

12:30 ~ 14:00 Lunch

14:00 ~ 16:00 Concurrency/Distributed Systems

Brijesh Dongol and Lindsay Groves
Contextual trace refinement for concurrent objects: Safety and progress

Madiel Conserva Filho, Marcel Vinicius Medeiros Oliveira, Augusto Sampaio and Ana Cavalcanti
Local Livelock Analysis of Component-Based Models

Tzu-Chun Chen, Crystal Chang Din and Eduard Kamburjan
Session-Based Compositional Analysis for Actor-Based Languages Using Futures

Badr Siala, Tahar Bhiri, Jean-Paul Bodeveix and Mamoun Filali-Amine
An Event-B development process for the distributed BIP framework

16:00 ~ 16:30 Coffee break

16:30 ~ 17:30 Panel Discussion

How can formal methods become effective and acceptable “medicine” for software engineering “diseases”?

18:00 ~ 21:30 Banquet (Symphony Tokyo Bay Dinner Cruise)

Friday, 18 November 2016

9:00 ~ 10:00 Keynote

Keijiro Araki
Promotion of Formal Approaches in Japanese Software Industry and a Best Practice of FeliCa's Case

10:00 ~ 10:30 Coffee break

10:30 ~ 12:30 Model Checking

Shuanglong Kan
Partial Order Reduction for State/Event Systems
Peizun Liu and Thomas Wahl
Concolic Unbounded-Thread Reachability via Loop Summaries

Truong Khanh Nguyen, Tian Huat Tan, Jun Sun, Jiaying Li, Yang Liu, Manman Chen and Jin Song Dong
Making Use of Simulation Techniques in Verifying Timed System

Mohammed Foughali, Bernard Berthomieu, Silvano Dal Zilio, Félix Ingrand and Anthony Mallet
Model Checking Real-Time Properties on the Functional Layer of Autonomous Robots

12:30 ~ 14:00 Lunch

14:00 ~ 15:30 Real-Time Systems

Étienne André, Didier Lime and Olivier H. Roux
Decision Problems for Parametric Timed Automata

Saurabh Gadia, Cyrille Valentin Artho and Gedare Bloom
Verifying Nested Lock Priority Inheritance in RT-EMS with Java Pathfinder

Min Zhang, Frederic Mallet and Huibiao Zhu
An SMT-based Approach to the Formal Analysis of MARTE/CCSL

15:30 ~ 16:00 Coffee break

16:00 ~ 17:00 Formal Analysis

Nuno Amalio, Richard Payne, Ana Cavalcanti and Jim Woodcock
Checking SysML Models for Co-Simulation

Manuel Toews and Heike Wehrheim
A CEGAR Scheme for Information Flow Analysis

17:00 ~ 17:15 Closing